```vhdl
--CONTADOR BCD A 7 SEGMENTOS
library ieee;
use ieee.std_logic_1164.all;
library cypress;
use cypress.std_arith.all;
--
entity cont7seg is port (
clk,reset: in std_logic;
D: out std_logic_vector(6 downto 0)); --salida del deco7seg
end cont7seg;
--
architecture arqcont7 of cont7seg is
signal Q: std_logic_vector(3 downto 0);  --salida del contador
begin
-- funcionamiento del contador
process (clk,reset) begin
if (clk 'event and clk='1') then Q<=Q+1;
        if (reset='1' or Q<="1001") then Q<="0000";
        end if;
end if;
end process;
--funcionamiento del decodificador
process (Q) begin
case Q is
        when "0000" => D<="1111110";
        when "0001" => D<="0110000";
        when "0010" => D<="1101101";
        when "0011" => D<="1111011";
        when "0100" => D<="0110011";
        when "0101" => D<="1011011";
        when "0110" => D<="1011111";
        when "0111" => D<="1110000";
        when "1000" => D<="1111111";
        when "1001" => D<="1110011";
        when others => D<="0000000";
end case;
end process;
end arqcont7;
```